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**REMARKS-General**

By the above amendments, applicants have amended the title to emphasize the novelty of the invention.

Also applicants have rewritten the claims 1, 6, and 8 to define the invention more particularly and distinctly so as to overcome the rejections and define the invention patentable over the prior art.

Applicant withdraws the original claims 9 to 23, the details is discussed below.

Applicant adds new claims 24 to 26 for second texture and second epitaxial layer emitting second wavelength light, which have be described in the original specification.

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**Election/restrictions and Response to amendment**

**Quote of the OA:**

"1. It is not clear exactly which are the claims that are respectively pending and withdrawn. For example, it is not appropriate to withdraw originally presented claims (such as claims 9-11) and present amended or new claims with the same claim numbers."

"For avoiding unnecessary delay in prosecution of the instant application, it is assumed in this office action that, in view of the amendment and election above, applicant intended to elect claims 1-11. Among them, claims 9-11 have been amended. And claims 12-23 are withdrawn from further consideration pursuant to 37 CFR1.142 as being drawn to a non-elected invention, there being no allowable generic or linking claim."

"In reply to this office action, applicant is required to confirm and/or clarify, with full list of claims along with their marked version, which claims are amended, and which claims are elected and which are withdrawn."

**Response:**

Applicant accordingly lists all of the claims: claim 1 is currently amended; claims 2 - 5 are the original claims; claim 6 is currently amended; claim 7 is the original claim; claim 8 is currently amended; claims 9 - 23 are withdrawn; claims 24 - 26 are new claims.

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**Drawings**

**Quote of the OA:**

"2. The drawings must show every feature of the invention specified in the claims. Therefore, the "shape" of the recited device as recited in claim 6 must be shown or the feature(s) canceled from the claim(s)."

"A proposed drawing correction or corrected drawings are required in reply to the office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance."

**Response:**

Applicant has amended claim 6 to avoid using "shape of device", and instead, using "shape of rectangular" for texture.

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### Claim Objection

#### Quote of the OA:

"3. Claims 1-11 are objected to because of the following informalities and/or defects:

Claim 1 recites the term of 'two surface', but fails to clarify what are the two surfaces. It appears that the term of 'one of its two surfaces' should read as : --a top surface of the substrate--."

#### Response:

Applicant has corrected the term in the currently amended claim 1 as the following: "a substrate with texture on the top surface of said substrate;"

#### Quote of the OA:

"In claim 8, the term of 'substrate' should read as: --device--, as the active layer is formed above the substrate."

#### Response:

Applicant has corrected the term in the currently amended claim 8 as the following: "The semiconductor device of claim 1, wherein said semiconductor device emits light."

#### Quote of the OA:

"Claim 9-11 recites the subject matters that a second texture formed on a first epitaxial layer that already comprises an active layer, implying that there are two active layers with the recited second texture there between. It apparently fails to reflect what is described in the specification, in which only one active layer for forming the recited devices is formed above the substrate."

#### Response:

Applicant requests reconsideration and withdrawal of the objection, because that applicant did describe two active layers for the recited device. The following is the quotation from the specification of the original patent application for FIG 7: "FIG. 7 shows a cross sectional view of epitaxial wafer. First texture comprising well 33 and wall 32 is etched on the top surface of substrate 31. First buffer layer 71 is grown on the first texture of substrate 31. First epitaxial layer 72 comprising first active layer is grown on the top surface of first buffer layer 71."

"Second texture comprising well 76 and wall 75 is patterned by etching on the top surface of first epitaxial layer 72. Second buffer layer 73 is grown on the second texture of first epitaxial layer 72. Second epitaxial layer 74 comprising second active layer is grown on the top surface of second buffer layer 73. Lights of different wavelength emitted from first epitaxial layer 72 and second epitaxial layer 74 are combined and emitted out of device."

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### Claim Rejections – 35 USC #112

#### Quote:

"Claim 6 is rejected under 35 USC 112, second paragraph, as being indefinite for failing to particular point out and distinctly claim the subject matter which applicant regards as the invention. Claim 6 recites the subject matter that the recited wells have the shape of the recited semiconductor device, but the disclosure lacks a clear description regarding what is the shape of the device. And, it is not clear how a well that is only a part of the device could have the shape

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of the whole device."

Response:

Prior to response to this rejection, applicant first explains the manufacturing process of semiconductor device. There are basically two steps in manufacturing semiconductor devices:

First step: designing:

1. designing the shape, size, and structure of the semiconductor device and the wafer fabrication process.
2. designing the structure and material system of the epitaxial layer and the epitaxial growth process.
3. choosing the growth substrate.

Second step: manufacturing:

1. preparing the growth substrate, in the present invention, further including forming texture on the top surface of the substrate.
2. growing the epitaxial layer on the substrate, in the present invention, the epitaxial layer is grown on the top of the texture.
3. wafer fabrication processing the substrate with the epitaxial layer on it and then cut the substrate into semiconductor devices with pre-determined shape and size.

One of ordinary skill in the art knows that the shape of semiconductor device is designed prior to grow the epitaxial layer. When texturing a substrate, the shape of the wells of the texture may have either the same shape as that of a pre-designed semiconductor device or different shapes. Thus a well that is only a part of the device may have the shape of the whole device, for example, for a square semiconductor device, the well may have the shape of square, for a rectangular shape semiconductor device, the well may have the shape of rectangular. On the other hand, the texture may not have the same shape as that of semiconductor device, for example, Wada in US 6797416 disclose a circular shaped texture, Asai in US 6426519 disclose a strip shaped texture.

The exact shape of semiconductor device is irrelevant to the present invention, since the present invention is about texturing a substrate and an epitaxial layer. Semiconductor devices may have any shape without having effect on texturing the substrate. Claim 6 of the applicant's patent application states that whatever shapes a semiconductor device has, the texture may have the same shape.

A daily life example is the following: making flower pattern on a wooden board (this step is equivalent to texturing wells on a substrate, flower corresponds to well), flowers may be very big or very small, glue a white paper onto the wooden board (this step is equivalent to grown buffer and epitaxial layers on the substrate). Then drawing squares on the white paper (each square corresponds to a semiconductor device). Then cut the wooden board along the lines of the square of the white paper to get individual square wooden board (this step is equivalent to dicing the substrate into semiconductor devices). The size of flower on the wooden board may be larger than, equal to, or smaller than the square on the white paper. If replacing the flower pattern with a square pattern, then the square on the wooden board may be larger than, equal to, or smaller than the square on the white paper. Although square pattern is part of wooden board, the square on the white paper may be larger than, equal to, or smaller than the square on the wooden board. The flower/square pattern on the wooden board is irrelevant with the square on the white paper.

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Applicant requests reconsideration and withdrawal of the rejection, because of the following reasons.

Applicant amends the claim 6 so that "said wells having a shape of rectangular".

Actually applicant has disclosed a rectangular shaped well as embodiments. Although applicant did not use the word "rectangular", the FIG 3 does show a rectangular shaped well and the specification does describe the width and length of the well. The width and length are associated with rectangular shape. See the following quotation of the applicant's patent application:

"FIG 3a is a cross sectional view of a preferred embodiment of the present invention. Texture comprising well 33 and wall 32 is patterned by etching on the top surface of substrate 31. Well 33 and well 34 are separated by wall 32. The depth of well 33 is in the range of nanometers to micrometers or thicker. The width and length of well 33 may be the same as device."

"FIG 3b is a top view of substrate 31 with patterns of well 33 and wall 32 on the top surface. Note the followings: (1) the shape of well is not limited to square and may be different, such as circle; (2) The width and length of well 33 may be different from that of device, even much smaller than that of device;"

A texture is formed on either a substrate or a GaN layer at wafer level and a 2 inch diameter substrate contains total of over 14,000 of semiconductor devices of dimension 0.3 x 0.275 mm. After wafer process, the substrate with the epitaxial layer on it will be cut into individual semiconductor devices. One of ordinary skill in the art knows that the size of texture may be larger than, equal to, or smaller than that of semiconductor device.

The semiconductor devices may have different shapes, for example square and rectangular shapes, depending on the manufacturing companies and product specifications. The present invention is devoted to the texture and texturing process and, thus, is applicable to all of different shapes, although, in the FIGs. of the patent application, applicant draws a rectangular shaped texture. Therefore applicant states that the well have the shape of semiconductor device without particularly stating the shape of the well.

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**Claim Rejections – 35 USC #102**

**Quote of the OA:**

"6 Claim 1-11, insofar as being in compliance with 35 USC 112 and as being best understood in view of the claim objections above, are rejected under 35 USC 102(e) as being anticipated by Wada et al (Wada, US 6,797,416)."

"Wada discloses a light emitting semiconductor device (FIGs. 1-7, especially FIGs 1B and 7; also see col. 2, lines 41-52), comprising: a first and a second textured layers 3 and 5 on a substrate 1; a buffer layer 2; and epitaxial layer/active layer 19-24 formed on the textured layer 5 wherein the textures in the textured layer comprises well 3b with walls therebetween, even having a dimension and a depth in microns".

"Regarding claim 6, it is noted that, insofar as being in compliance with 35 USC 112, the

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wells in Wada becomes a part of the device's cross-section shape."

**Response:**

Applicant requests reconsideration and withdrawal of the rejection, because the current amended claims 1, 6, and 8, the original claims 2 to 5, and 7, and the new claims 24 to 26 distinguish over Wada's invention under 35 USC 102(e) for the following reasons.

- (1) The novel physical structure of the semiconductor device of the amended claims 1, 6, and 8, the original claims 2 to 5 and 7, and the new claims 24, 25, and 26 of the present patent application distinguishes over Wada's patent.
- (2) These novel physical structures of the amended claims 1, 6, and 8, the original claims 2 to 5 and 7, and the new claims 24, 25, and 26 of the present patent application produce new and unexpected results and hence are unobvious and patentable over Wada's patent.

These 2 points will be discussed in detail below.

**The references and Differences of the present patent application thereover.**

Prior to discuss the claims and the above 2 points, applicant will first discuss the Wada's patent and the general novelty of the present patent application and its unobviousness over Wada's patent.

There are several criterions to distinguish semiconductor devices with textures:

- (1) the physical structure;
- (2) how many active layers a semiconductor device has,;
- (3) in what sequence the texture, the buffer layer and the epitaxial layer grow.

The present patent application is classified in a crowded art, therefore even a small step forward should be regarded as significant, especially a novel physical structure definitely distinguishes over prior art.

Wada et al disclose, in the cited prior patent 6,797,416, a semiconductor device comprising the following key characteristics elements:

- (a) A semiconductor device comprising a buffer layer 2 (Wada calls it the GaN buffer layer 2) grows on base substrate 1. The first GaN layer 3 is grown on the upper surface of GaN buffer layer 2. The texture (Wada calls it the pit) is formed on the upper surface of the first GaN layer 3, as shown below:

Epitaxial layer: <u>active layer</u>
GaN buffer layer 7
Second GaN layer 5 <u>with pits</u>
First GaN layer 3 <u>with pits</u>
GaN Buffer layer 2
Base substrate 1

FIG. 1d of Wada's patent

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The following are quotations from Wada's patent: "As illustrated in FIG 1D, the substrate for use in a semiconductor element, in the first embodiment of the present invention, comprises a base substrate 1, a GaN buffer layer 2 formed on the base substrate 1, a first GaN layer 3 being formed on the GaN buffer layer 2 and having a plurality of pits 3b at its upper surface, and a second GaN layer 5 formed by growing a GaN crystal over the first GaN layer 3 until the upper surface of the second GaN layer 5 becomes flattened."

"First, as illustrated in FIG. 1a, a GaN buffer layer 2 is formed on a (0001) face of a sapphire substrate 1 (as the base substrate) at a temperature of 500 degree C."

"Then a first GaN layer 3 having thickness of about 2  $\mu\text{m}$  is formed on the GaN buffer layer 2 at a temperature of 1050."

"Next, as illustrated in FIG. 1b, a SiO<sub>2</sub> layer 4 having a thickness of 0.5  $\mu\text{m}$  is formed on the first GaN layer 3 by plasma CVD using SiH<sub>4</sub> gas and N<sub>2</sub>O gas, and a resist film in which a plurality of openings are patterned by photolithography is formed on the SiO<sub>2</sub> layer 4, where each of the plurality of openings having a round shape with a diameter of 2  $\mu\text{m}$  are arranged....Subsequently, the SiO<sub>2</sub> film 4 is etched by RIE dry etching using CHF<sub>3</sub>/O<sub>2</sub> gas as an etchant and the above resist pattern as a mask, and the resist pattern is removed by the O<sub>2</sub> plasma ashing technique. Thus the SiO<sub>2</sub> film 4 becomes a pattern having a plurality of round opening 4a."

"Thereafter, as illustrated in FIG. 1c, a plurality of portions of the first GaN layer 3 exposed through the plurality of opening 4a of the SiO<sub>2</sub> film 4 are etched to a depth of 1  $\mu\text{m}$  by the ECR(electron cyclotron resonance) etching using Cl<sub>2</sub> gas as an etchant and the SiO<sub>2</sub> film as a mask, and then the SiO<sub>2</sub> film 4 is removed with hydrofluoric acid. Thus a plurality of pits 3b each has a cylindrical shape with a diameter of 2  $\mu\text{m}$  and depth of 1  $\mu\text{m}$  are formed."

"Further, as illustrated in FIG. 1d, a crystal of a second GaN layer 5 is grown over the first GaN layer at a growth temp 1080 degree C by MOVPE, so that the upper portion of each of the plurality of pits 3b is closed by lateral growth and the upper surface of the second GaN layer 5 becomes flattened. Since the growth temp is relatively high (1080 C), the growth speed in the lateral directions are greater than the growth speed in the vertical direction. Therefore the second GaN layer 5 grows so as to fill the plurality of pits 3b in the first GaN layer 3."

"It is possible to form a plurality of pits 5b at the upper surface of the second GaN layer 5 (as illustrated in FIG. 2a), and grow a third GaN layer 7 over the second GaN layer 5 until the upper surface of the third GaN layer 7 becomes flattened (FIG.2b)."

To show clearly the distinctions between Wada and applicant, comparing with FIG. 7 of the applicant's patent application, shown as below:

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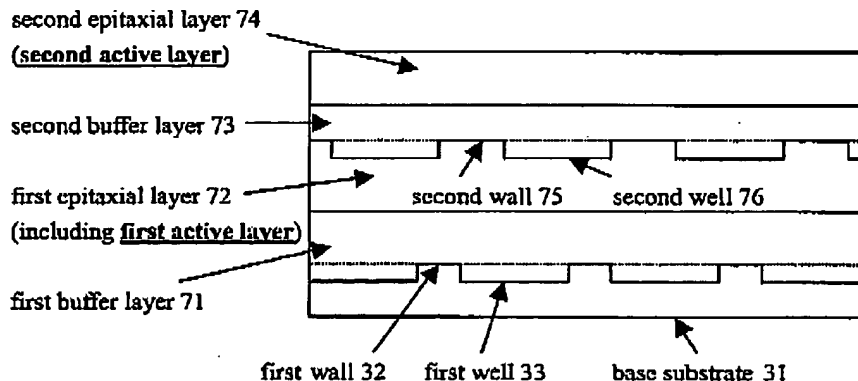


FIG. 7 of the applicant's patent application

Now discuss the above 2 points and what novel features applicant discloses and claims:

(1) The novel physical structure of the semiconductor device of the amended claims 1, 6, and 8, the original claims 2 to 5 and 7, and the new claims 24, 25, and 26 of the present patent application distinguishes over Wada's patent.

One of ordinary skill in the art knows that Applicant's invention distinguish over Wada's invention, since the following:

(1) Wada's first texture (first pits) is formed on the upper surface of the first GaN layer 3. Wada et al clearly indicate in their claims 1, 2, 3, 4, 5, and 6 that "forming a first GaN layer having a plurality of pits at an upper surface of the first GaN layer."

The applicant's texture is directly formed on the base substrate 1. Applicant clearly indicates in claim 1 that "A semiconductor device, comprising a substrate with texture on the top surface of said substrate."

(2) Wada's second texture (second pits) is formed on the upper surface of the second GaN layer 5. The second GaN layer 5 is grown on first GaN layer 3 and does not including an active layer. Actually Wada did not claim second pits in their claims.

Applicant's second texture is formed on the first epitaxial layer which including a first active layer. Applicant clearly indicates in new claim 24 that "The semiconductor device of claim 1, further comprises a second texture formed on the top of said epitaxial layer."

(3) there is only one active layer in Wada's patent (see FIG. 7 of Wada's patent). Actually Wada did not claim the active layer in their claims.

There are two active layers emitting two lights of different wavelengths in applicant's patent application. Applicant clearly indicates in new claim 25 that "The semiconductor device of claim 24, further comprises a second epitaxial layer grown on the top of said second texture and comprising a second active layer."

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The followings are the applicants' response to the OA.

It was said in the Office Action Summary (hereafter called it OA) that "Wada discloses a light emitting semiconductor device (FIGs. 1-7, especially FIGs 1B and 7; also see col. 2, lines 41-52), comprising: a first and a second textured layers 3 and 5 on a substrate 1; a buffer layer 2; and epitaxial layer/active layer 19-24 formed on the textured layer 5"

This statement of the OA describes "a first and a second textured layers 3 and 5 on a substrate 1". Comparing with Wada's claims and specification, the above statement of the OA is not exactly what Wada et al disclose and claim.

Wada et al clearly indicate in the specification that "a GaN buffer layer 2 formed on the base substrate 1, a first GaN layer 3 being formed on the GaN buffer layer 2 and having a plurality of pits 3b at its upper surface" and in the claims 1, 2, 3, 4, 5, and 6 that "(a) forming a first GaN layer having a plurality of pits at an upper surface of the first GaN layer."

Therefore the first texture (pits) of Wada's invention is not formed on a base substrate.

The texture of applicant's invention is formed on a base substrate.

(2) These novel physical structures of the amended claims 1, 6, and 8, the original claims 2 to 5 and 7, and the new claims 24, 25, and 26 of the present patent application produce new and unexpected results and hence are unobvious and patentable over Wada's patent.

This different in structure makes big different in production process and cost: for comparing applicant's invention with Wada's invention, only consider semiconductor device with one active layer, since Wada's invention has only one active layer. One of ordinary skill in the art knows that a semiconductor device with two active layers is a significantly different subject matter from that with one active layer.

The process for manufacturing Wada's device is the following (for detail, please see the quotation for the FIG 1 of Wada's patent above):

1. Growing buffer layer 2 and first GaN layer 3 on the substrate in MOVPE equipment;
2. taking the substrate with buffer layer 2 and first GaN layer 3 on it out of MOCVD equipment, forming a SiO<sub>2</sub> layer on the first GaN layer in plasma CVD equipment;
3. plurality of openings patterned by photolithography is formed on the SiO<sub>2</sub> layer 4;
4. the SiO<sub>2</sub> film 4 is etched by RIE dry etching
5. plurality of portions of the first GaN layer 3 exposed through the plurality of opening 4a of the SiO<sub>2</sub> film 4 are etched to a depth of 1 um by the ECR(electron cyclotron resonance) etching;
6. the SiO<sub>2</sub> film 4 is removed
7. placing the substrate into MOVPE equipment again, a second GaN layer 5 is grown over the first GaN layer at a growth temp 1080 degree C.

The process for manufacturing applicant's device is the following:

1. etching well texture on the substrate
2. place the substrate into MOVPE equipment and grow buffer layer, and other epitaxial layers.

Now it is obvious that the new and unexpected results of applicant's invention over Wada's invention are the following.



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For semiconductor device having one active layer: in applicant's invention, the substrate is placed into MOVPE once until the growth of the semiconductor device's epitaxial layer is completed. In Wada's invention the substrate is placed into MOVPE twice. One of ordinary skill knows that Wada's process is more complex, costly, easy to be contaminated, and the first GaN layer 3 is easy to be damaged by the processes of texturing the first GaN layer thereon.

For semiconductor device having two active layers: in applicant's invention, there are two active layers and thus may emit white light or desired color light by combination of two different wavelength lights. In Wada's invention, there is only one active layer, and thus only emit a single wavelength light.

It is the differences in detail structures of semiconductor device with texture and different number of active layers that distinguish applicants over Wada.

Applicants' semiconductor devices therefore are vastly superior to that of Wada et al. The novel features of applicants' LEDs which effect these differences are, as stated, clearly recited in the amended claims 1, 6, and 8, and the original claims 2 to 5 and 7, and new claims 24 to 26.

Quote of the OA:

"Regarding claim 11, at least layer 7 is readable as the recited second buffer layer."

Response:

Even if Wada's layer 7 is readable as the recited second buffer layer, there are still significant differences between Wada and applicant as the following: there is no active layer inbetween Wada's first and second buffer layer, both Wada's first and second textures and first and second buffer layer. There is the first active layer inbetween Applicant's first and second buffer layer.

Therefore applicant's invention is distinct over Wada's invention.

Brief:

Thus the specification, the amended claims 1, 6, and 8, and original dependent claims 2 to 5 and 7, and new claims 24 to 26 of the present patent application clearly and strongly distinguish over Wada's patent in novel physical structures, manufacturing process and cost, and produce new and unexpected results and hence are unobvious and patentable.

Accordingly the applicants submit that the specification and claims do comply with 35 USC 102 and therefore request withdrawal of the rejection.

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Conclusion

Quote of the OA:

"The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference B-I are cited for being related to a substrate for lateral-epitaxial growth of active layer thereon."

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**Response:**

As shown above, applicant invention is clearly and strongly distinguish over Wada's patent.

It is not clear what are "Reference B-I". For avoiding unnecessary delay in prosecution of the instant application, it is assumed in this amendment A, that the OA intended to use references cited in "Notice of reference cited" as a combination to reject applicant's invention under 35 USC 103. therefore applicant responses to the OA for those references as the following.

**under 35 USC 103**

The OA references additional 8 of US patents in the "Notice of References Cited".

Although the OA did not employ the 35USC 103 to reject the applicant's invention by combining the references cited in the "Notice of References Cited", applicant would like to state the following reasons why the distinctions of the applicant's invention were over Wada's patent in view of other references cited in "Notice of References Cited".

**(1) Wada et al and other reference Do Not Contain Any Justification to Support Their Combination.**

With regard to the combination of Wada and other references, it is well known that in order for any prior art references themselves to be validly combined for use in a prior art 35 USC 103 rejection, the *references themselves* (or some other prior art) must suggest that they be combined. For example, as was stated in In re Sernaker, 217 U.S.P.Q. 1, 6 (C.A.F.C.1983):

"Prior art references in combination do not make an invention obvious unless something in the prior art references would suggest the advantages to be derived from combining their teachings."

That the suggestion to combine the references should not come from applicants was forcefully stated in Orthopedic Equipment Co. v. United States, 217 U.S.P.Q 193, 199 (C.A.F.C 1983):

"it was wrong to use the patent in suit [here the patent application] as a guide through the maze of prior art references, combining the right references in the right way to achieve the result of the claims in suit [here the claims pending]. Monday morning quarterbacking is quite improper when resolving the question of non-obviousness in a court of law [here the PTO]."

As was further stated in Uniroval Inc. v. Rudkin-Wiley Corp., 5 U.S.P.Q.2d 1434 (C.A.F.C. 1988):

".....Something in the prior art must suggest the desirability and thus the obviousness of making the combination."

In line with this decisions, recently the Board stated in Ex parte Levengood, 28 U.S.P.Q.2d 1300 (P.T.O.B.A.&I. 1993):

" In order to establish a prima facie case of obviousness, it is necessary for the examiner to present evidence, preferably in the form of some teaching, suggestion, incentive or inference in the applied prior art, or in the form of generally available knowledge, that one having ordinary skill in the art would have been led to combine the relevant teaching of the applied references in the proposed manner to arrive at the claimed invention....Our reviewing

**Brief:**

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Thus applicants submit that the applicant's invention clearly recite novel physical subject matters including physical structures, which distinguish over any possible combination of Wada and other references, and produce new and unexpected results and hence are unobvious and patentable over any combination of Wada's and other patents under section 35 USC 103.

**CONCLUSION**

For all the above reasons, applicants submit that the specification and claims are now in proper form, and that the claims all define patentable over the prior art. Therefore applicant submits that this application is now in condition for allowance, which action they respectfully solicit.

**Conditional Request for Constructive Assistance**

Applicants have amended the specification and claims of this application so that they are proper, definite, and define novel structure, which is also unobvious. If, for any reason this application is not believed to be in full conditions for allowance, applicants respectfully request the constructive assistance and suggestions of the Examiner pursuant to M.P.E.P. Section 2173.02 and section 2173.07(j) in order that the undersigned can place this application in allowable condition as soon as possible and without the need of further proceedings.

Very respectfully

Hui Peng

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Certificate of Mailing. I certify that, on the date below, this correspondence will be deposited with the United State Postal Service by First Class Mail, postage prepaid, in an envelop addressed to "Box Non-Fee Amendments, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450", and faxed to 703-872-9306.

Date: Feb. 17, 2005

Inventor's signature: H. Peng